



PTO/SB/21 (09-04)

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**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	10/699,116
Filing Date	October 31, 2003
First Named Inventor	Donnelly
Art Unit	2187
Examiner Name	Chace, C.
Attorney Docket Number	RAMB-01065US1

ENCLOSURES (Check all that apply)

- | | | |
|---|--|---|
| <input checked="" type="checkbox"/> Fee Transmittal Form
<input checked="" type="checkbox"/> Fee Attached
<input type="checkbox"/> Amendment/Reply
<input type="checkbox"/> After Final
<input type="checkbox"/> Affidavits/declaration(s)
<input type="checkbox"/> Extension of Time Request
<input type="checkbox"/> Express Abandonment Request
<input checked="" type="checkbox"/> Information Disclosure Statement

<input type="checkbox"/> Certified Copy of Priority Document(s)
<input type="checkbox"/> Reply to Missing Parts/
Incomplete Application
<input type="checkbox"/> Reply to Missing Parts
under 37 CFR 1.52 or 1.53 | <input type="checkbox"/> Drawing(s)
<input type="checkbox"/> Licensing-related Papers

<input type="checkbox"/> Petition
<input type="checkbox"/> Petition to Convert to a
Provisional Application
<input type="checkbox"/> Power of Attorney, Revocation
Change of Correspondence Address

<input type="checkbox"/> Terminal Disclaimer

<input type="checkbox"/> Request for Refund

<input type="checkbox"/> CD, Number of CD(s) _____
<input type="checkbox"/> Landscape Table on CD | <input type="checkbox"/> After Allowance Communication to TC

<input type="checkbox"/> Appeal Communication to Board
of Appeals and Interferences

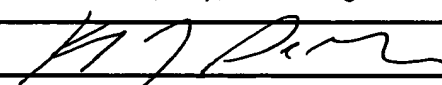
<input type="checkbox"/> Appeal Communication to TC
(Appeal Notice, Brief, Reply Brief)

<input type="checkbox"/> Proprietary Information

<input type="checkbox"/> Status Letter
<input checked="" type="checkbox"/> Other Enclosure(s) (please identify
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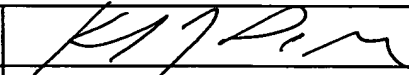
Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Kirk J. DeNiro, Esq., Vierra Magen Marcus Harmon & DeNiro LLP
Signature	 3/15/05
Printed name	Kirk J. DeNiro
Date	March 15, 2005
Reg. No.	35,854

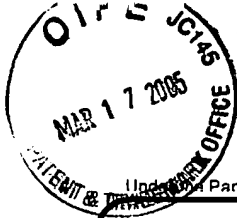
CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature	 3/15/05
Typed or printed name	Kirk J. DeNiro
Date	March 15, 2005

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Effective on 12/08/2004.

Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL

For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 180.00

Complete if Known

Application Number	10/699,116
Filing Date	October 31, 2003
First Named Inventor	Donnelly
Examiner Name	Chace, C.
Art Unit	2187
Attorney Docket No.	RAMB-01065US1

METHOD OF PAYMENT (check all that apply)☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): Vierra Magen Marcus☒ Deposit Account Deposit Account Number: Harmon & DeNiro LLP Deposit Account Name: 501826

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below☐ Charge fee(s) indicated below, except for the filing fee☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES**Fee Description**

Each claim over 20 (including Reissues)

Fee (\$)

Small Entity Fee (\$)

50

25

Each independent claim over 3 (including Reissues)

200

100

Multiple dependent claims

360

180

Total Claims	Extra Claims	Fee (\$)	Fee Paid (\$)
- 20 or HP =	x	50	= 0

Multiple Dependent Claims	Fee (\$)	Fee Paid (\$)
- 3 or HP =	x	200

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee (\$)	Fee Paid (\$)
- 3 or HP =	x	200	= 0

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
- 100 =	/ 50 =	(round up to a whole number) x		

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Fees Paid (\$)

Other (e.g., late filing surcharge): Information Disclosure Statement fee

180

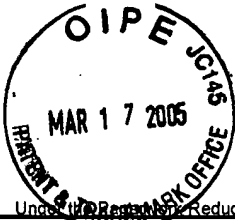
SUBMITTED BY

Signature	<u>[Signature]</u>	Registration No. (Attorney/Agent) 35,854	Telephone 415-369-9660
Name (Print/Type)	Kirk J. DeNiro	3/15/05	Date March 15, 2005

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1

of 7

Complete if Known

Application Number	10/699,116
Filing Date	October 31, 2003
First Named Inventor	Donnelly
Art Unit	2187
Examiner Name	Chace, C.
Attorney Docket Number	RAMB-01065US1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US-6016282	1-18-2000	Keeth	
		US-6449727	09-10-2002	Toda	
		US-4644532	02-17-1987	George et al.	
		US-4667305	05-19-1987	Dill et al.	
		US-4747100	05-24-1988	Roach et al.	
		US-4864563	09-05-1989	Pavey et al.	
		US-5228134	07-13-1993	MacWilliams et al.	
		US-5355467	10-11-1994	MacWilliams et al.	
		US-5408646	04-18-1995	Olnowich et al.	
		US-5537394	07-16-1996	Abe et al.	
		US-5544342	08-06-1996	Dean	
		US-5553266	09-03-1996	Metzger et al.	
		US-5557266	09-17-1996	Calvignac et al.	
		US-5604735	02-18-1997	Levinson et al.	
		US-5630095	05-13-1997	Snyder	
		US-5659710	08-19-1997	Sherman et al.	
		US-5787083	07-28-1998	Iwamoto et al.	
		US-5802054	09-01-1998	Bellenger	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁵
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
		WO 99/30240	06-17-1999	Intel Corporation		
		WO 99/41666	08-19-1999	Intel Corporation		
		WO 99/41667	08-19-1999	Intel Corporation		
		EP 1069509 A2	01-17-2001	Texas Instruments Incorporated		

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**INFORMATION DISCLOSURE
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Sheet 2

of 7

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First Named Inventor	Donnelly
Art Unit	2187
Examiner Name	Chace, C.
Attorney Docket Number	RAMB-01065US1

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		Number-Kind Code ² (if known)			
		US-5802565	09-01-1998	McBride	
		US-5805798	09-08-1998	Kearns et al.	
		US-5848145	12-08-1998	Gallagher et al.	
		US-5884036	03-16-1999	Haley	
		US-5893921	04-13-1999	Bucher et al.	
		US-5900017	05-04-1999	Genduso et al.	
		US-5901294	05-04-1999	Tran et al.	
		US-5911052	06-08-1999	Singhal et al.	
		US-5913044	06-15-1999	Tran et al.	
		US-5923893	07-13-1999	Moyer et al.	
		US-6247100	06-12-2001	Drehmel et al.	
		US-5953215	09-14-1999	Karabatsos et al.	
		US-6142830	11-07-2000	Looeffler	
		US-6185644	02-06-2001	Farmwald et al.	
		US-6266252	07-24-2001	Karabatsos	
		US-6317352	11-13-2001	Halbert et al.	
		US-6414904	07-02-2002	So et al.	
		US-6446158	09-03-2002	Karabatsos	

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Sheet 3

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		Number-Kind Code ² (if known)			
		US-6493250	12-10-2002	Halbert et al.	
		US-6530006	03-04-2003	Dodd et al.	
		US-6449679	09-10-2002	Ryan et al.	
		US-6108731	08-22-2000	Suzuki et al.	
		US-5701313	12-23-1997	Purdham	
		US-5513135	04-30-1996	Dell et al.	
		US-6065092	05-16-2000	Roy	
		US-5034917	07-23-1991	Bland et al.	
		US-4977498	12-11-1990	Rastegar et al.	
		US-5068650	11-26-1991	Fernandez et al.	
		US-4947257	08-07-1990	Fernandez et al.	
		US-6643752	11-04-2003	Donnelly et al.	
		US-6690726	02-10-2004	Yavits et al.	
		US-5325493	06-28-1994	Herrell et al.	
		US-5867180	02-02-1999	Katayama et al.	
		US-6104417	08-15-2000	Nielsen et al.	
		US-6208273	03-27-2001	Dye et al.	
		US-5883839	03-16-1999	Tosaka et al.	

FOREIGN PATENT DOCUMENTS

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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

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Sheet 4

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		Number-Kind Code ² (if known)			
		US-20040260991	12-23-2004	Vogt et al.	
		US-20040250181	12-09-2004	Vogt et al.	
		US-20040250153	12-09-2004	Vogt	
		US-20040150024	12-09-2004	Vogt	
		US-20040246786	12-09-2004	Vogt	
		US-20040246785	12-09-2004	Vogt	
		US-20040246767	12-09-2004	Vogt	
		US-20040015650	01-22-2004	Zumkehr et al.	
		US-20030177313	09-18-2003	Iyer et al.	
		US-20020083287	06-27-2002	Zumkehr et al.	
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**INFORMATION DISCLOSURE
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(Use as many sheets as necessary)

Sheet

5

of

7

Complete if Known

Application Number

10/699,116

Filing Date

October 31, 2003

First Named Inventor

Donnelly

Art Unit

2187

Examiner Name

Chace, C.

Attorney Docket Number

RAMB-01065US1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Intel Developer Forum, "DDR2 Memory In 2004 Servers - Recipes For Successful Designs", September 2003	
		QBM Alliance, Platform Conference, "Quad Band Memory (QBM tm): DDR 200/266/333 devices producing DDR400/533/667, Jan. 23-24, 2002	
		KARABATSOS, C., "Quad Band Memory (QBM) Technology", Kentron Technologies, Inc., April 2001	
		Quad Band Memory (QBM), "The 'QBM Enabled' VIA PT880/PM880 Chipset Solutions with the Fastest Memory",	
		WEBER, F., "The AMD Athlon Processor: Future Directions", AMD	
		"Intel 82804AA Memory Repeater Hub for SDRAM (MRH-S) Datasheet", Intel Corp., pp. 2-48 (Nov. 1999)	
		"Intel 82805AA Memory Translator Hub (MTH) Datasheet", Intel Corp., pp. 1-48 (Nov. 1999)	
		CATALDO, A., "TI Fields DSP-Based Media Processor on a DIMM", EE Times (Jan. 2000)	
		MAC WILLIAMS, P., "PC Memory Directions For 1999 and Beyond", Intel Developer Forum, pp. 1-10 (Sep. 1998)	
		JOHNSON, B., "Direct RDRAM Basic Architecture and Program Overview", Intel Developer Forum, pp. 1-14 (Sep. 1998)	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	10/699,116
Filing Date	October 31, 2003
First Named Inventor	Donnelly
Art Unit	2187
Examiner Name	Chace, C.
Attorney Docket Number	RAMB-01065US1

Sheet 6 of 7

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		GILLINGHAM, P., "SLDRAM Architectural and Functional Overview", SLDRAM Consortium, SLDRAM Inc., pp. 1-14 (Aug. 1997)	
		"Draft Standard for a High-Speed Memory Interface (Synclink)", Draft 0.99 IEEE P1596.7-199X, IEEE Inc., pp. 1-51 (1996)	
		WIGGERS, H., "SyncLink A Proposal for an Implementation of IEEE P1596.4", Hewlett Packard, pp. 1-20 (Mar. 1995)	
		"KMM377S1620CT2 SDRAM Module Datasheet", Samsung Electronics Inc., pp. 1-2 (Nov. 1998)	
		"SLD4M18DR400 4MEG x 18 SLDRAM Datasheet", SLDRAM Inc., pp. 1-69 (July 1998)	
		POULTON, J., "Signaling in High Performance Memory Systems", IEEE Solid State Circuits Conference, slides 1-59 (Feb. 1999)	
		"SLDRAM 400Mb/s/pin Command/Address Repeater", SLD10400 Rev .5, SLDRAM Consortium, pp. 1-12 (Jan. 7, 1998)	
		Minutes of meeting no. 75 JEDEC JC-42.3 Committee on RAM Memories, and referenced attachment "Y" of the presentation titled "SyncLink", May 24, 1995, New Orleans	
		Intel Developer Forum, "Fully Buffered DIMM (FB-DIMM) Server Memory Architecture: Capacity, Performance, Reliability, and Longevity", February 18, 2004	
		Intel Developer Forum, "Fully Buffered DIMM (FB-DIMM) Design Considerations", February 18, 2004	

Examiner Signature	Date Considered
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Sheet 7 of 7**Complete if Known**

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		IEEE Standard for Scalable Coherent Interface (SCI), "Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society", IEEE Std 1596-1992	
		SCI, "P1596: SCI, A Scalable Coherent Interface", November 28, 1988	
		GUSTAVSON et al., DRAFT "The Scalable Coherent Interface Project (SuperBus)", SCI, August 22, 1988, Rev. 14	
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		JAMES, "Scalable I/O Architecture for Buses", COMPCON Spring 1989, SCI, November 28, 1988	
		VOLZ et al., "Position Paper On Global Clock For the Futurebus +", SCI, 1989	
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		GUSTAVSON et al., "Macintosh HD:Desktop Folder:SLDRAMrepeaterConcerns", Sunday, November 23, 1997, 4 pages	
		JEDDELOH, JOE, "Fully Buffered DIMM (FB-DIMM)", Advanced Systems Technology, Micron Technology, Inc. April 15-16, 2004	

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